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PATENT APPLICATION

METHOD FOR IMPROVED LOCAL PLANARITY CONTROL DURING ELECTROPOLISHING

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METHOD FOR IMPROVED LOCAL PLANARITY CONTROL DURING ELECTROPOLISHING

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to methods for performing polishing of semiconductor wafers. More particularly, the present invention relates to methods for mechanical stress free processing of damascene interconnects on semiconductor wafers during the manufacture of semiconductor integrated circuits.

2. Description of the Related Art

As integrated circuits become smaller, it becomes more desirable to reduce interconnection delays through the selection of materials used in the interconnects and associated dielectric layers. The propagation delays through the interconnects are proportional to the resistance of the interconnects and the capacitance offered by the dielectric. In fact, as integrated devices become smaller, the resistance capacitance (RC) delay time of signal propagation along interconnects becomes the dominant factor limiting overall chip speed. In order to improve the interconnect performance, higher conductance and lower capacitance is required of the interconnects. In order to accommodate these objectives, the trend has been towards the use of copper for interconnects and damascene methods for forming the interconnects.

For conductors, copper has gained favor in the industry because of its many advantages, including its low resistance. In such processes, conducting metal (e.g., copper) is inlaid into trench and via structures of insulating material (e.g., low-k dielectric materials). CMP (Chemical Mechanical Polishing) is typically used to remove conducting metal (e.g., copper) in single or dual damascene processes. With the advent of copper technology, resistance has been minimized and attention has been focused on reducing capacitance.

One method conventionally used to reduce capacitance is to reduce the average dielectric constant k of the thin insulating films surrounding interconnects through the introduction of porosity. The dielectric layers in conventional integrated circuits have traditionally been formed of SiO_2, which has a dielectric constant of about 4.0. A number of dielectric materials have been developed having a dielectric constant lower than that of SiO_2. These are generally referred to as low-k materials.

But low-k materials used in interconnect dielectrics exhibit low mechanical strength. This compromised mechanical strength of the low-k film significantly increases the likelihood of damage to the structure of the low-k copper dual damascene system during conventional chemical mechanical polishing (CMP). That is, while the wafers are subjected to chemical mechanical polishing (CMP), shear stresses and other mechanical damage may cause defects in the devices. The poor mechanical strength and the adhesion properties may result in delamination and/or line breakage, due to applied stress during conventional chemical mechanical polishing (CMP) in typical damascene

integration schemes. Additional challenges presented by the CMP steps include unwanted erosion and dishing on the planarized surface. Thus, the poor mechanical strength of the low-k material affects the ability to use chemical mechanical polishing to remove the copper film and planarize the wafer surface between copper layers.

Stress-Free-Polishing (SFP) has been proposed to overcome these problems. Stress-free polishing uses electrochemical principles to "isotropically" de-plate (remove) the deposited Cu layer in order to form the planarized surface. Unfortunately, SFP processes poorly control the within-feature dishing characteristics.

The uneven within-feature dishing characteristics results from the local topography (or pattern) induced electric field variation, resulting in uneven distribution of de-plating rates. Since the electrochemical de-plating (or plating) rates vary exponentially with respect to the applied potential when the potential is greater than the required minimum voltage, small variations in potential produce significant changes in the plating or de-plating rates. Since the electrical field is highest at sharp points, for example, at the feature corners in a typical damascene interconnect structure, the de-plating rate is highest around those corners, resulting in deeper dishing at those corners.

Accordingly, it is desirable to provide improved stress-free-polishing methods of planarizing semiconductor wafer surfaces to minimize or eliminate damage to dielectric layers. In particular, it is desirable to provide more effective methods of

stress-free polishing to produce planarized surfaces in low-k damascene interconnect structures and to avoid dishing characteristics and other unwanted characteristics in the planarized surfaces.

SUMMARY OF THE INVENTION

To achieve the foregoing, the present invention provides methods for processing semiconductor wafers using a stress-free polishing method using a combination of electroplating and electropolishing. Planarization is accomplished by a sequence of electroplating/electropolishing/relaxation cycles, each of the electroplating or electropolishing steps followed by a relaxation period. In order to avoid topography dependant electropolishing, the plating solution contains organic additives to induce the local topography-dependant plating rates. The processing sequence involves an initial electropolishing step in conjunction with an electroplating step. Initially the ratio of the electropolishing rate to the electroplating rate is greater than 1 to reflect the presence of the blanket copper layer recently deposited. As the barrier layer and the underlying dielectric layer becomes exposed, the ratio is gradually reduced in subsequent passes until a ratio of 1 is present when the desired Cu dishing characteristics are achieved.

By processing the semiconductor wafer in this manner, a non-contact method of removing copper from the wafer is provided.

According to one embodiment, a method of planarizing a surface of a semiconductor substrate is provided. A metal layer formed on a semiconductor wafer is planarized by applying sequentially a deplating step, a plating step, and a relaxation step in a series of removal cycles. The removal cycle is repeated as necessary to complete the first pass. The respective deplating and plating rates are adjusted so that

the ratios of deplating rates to plating rates progressively decrease from the initial pass to the final pass. Organic additives are added to the electrolytic plating solution to control the plating portion of the cycle in a topography dependant fashion.

These and other features and advantages of the present invention are described below with reference to the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagrammatic view of a trench using conventional electropolishing methods.

FIG. 2 is a diagram illustrating a trench polished in accordance with one embodiment of the present invention.

FIG. 3 is a flowchart illustrating a method of polishing a substrate surface in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Reference will now be made in detail to preferred embodiments of the invention. Examples of the preferred embodiments are illustrated in the accompanying drawings. While the invention will be described in conjunction with these preferred embodiments, it will be understood that it is not intended to limit the invention to such preferred embodiments. On the contrary, it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. The present invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to unnecessarily obscure the present invention.

To achieve the foregoing, the present invention provides methods for processing semiconductor wafers using a stress-free polishing method using a combination of electropolishing and electroplating. Planarization is accomplished by a sequence of electroplating/electropolishing cycles, each of the electroplating or electropolishing bursts or pulses followed by a relaxation period. In order to avoid topography dependant electropolishing, the plating solution contains organic additives to induce the local topography-dependant plating rates. The processing sequence involves an initial electropolishing step in conjunction with an electroplating step.

During the initial pass, the ratio of the electropolishing rate to the electroplating rate is greater than 1 to reflect the presence of the blanket copper layer recently deposited. As the barrier layer becomes exposed, the ratio is gradually reduced until a ratio of 1 is present when the desired Cu dishing characteristics are achieved.

As discussed above, with increasing miniaturization of integrated circuits, the trend has been towards incorporating copper interconnect metal layers with low-k dielectric layers in forming the interconnect levels for these circuits. These interconnect layers are typically formed by damascene methods. For example, damascene processing involves etching trenches in insulating layers (such as a low-k layer) in a desired pattern for a wiring layer. These trenches are then filled with conductive material to produce the integrated interconnect wires. Where contact vias, extending downwardly from the bottom of the trenches, are simultaneously filled, the process is known as dual damascene. The fill process for the copper interconnects typically includes a diffusion barrier, a copper seed layer, and the deposition of the bulk copper. The copper interconnect lines are formed by polishing away the field copper, the seed layer, and the diffusion barrier down to the underlying dielectric.

The softer and more porous low-k dielectrics are generally unable to withstand the extreme stresses created by chemical mechanical polishing. Chemical mechanical polishing (CMP) creates problems such as scratching, peeling, and dishing that are exacerbated when performed on interconnects formed from the low-k dielectrics and copper.

The present invention overcomes these problems by cycling electropolishing with electroplating, and controlling the topography dependant rates of each by the use of chemical additives.

Electropolishing ("deplating") is an electrochemical process that typically removes defects from the surface of a metal part using a combination of rectified current and a chemical electrolyte in which the metal part is immersed. In particular, the metal part to be polished is connected to a positive voltage to form an anode. Large DC currents flow from the anode to a metal cathode to perform an operation that has been described as the reverse operation of electrochemical deposition ("electroplating"). As used herein, the electrochemical deposition process is also referred to as "electroplating" or "plating". In deplating, the currents produce electric fields to provide increased metal removal rate over the microscopic peaks of the metal part, resulting in smooth surfaces at efficient removal rates.

With the arrangement as disclosed, the same electrolytic solution is used for electropolishing and electroplating. Thus, the same tool may be used to perform a cycle of plating and polishing to facilitate planarization of the wafer surface by combined electroplating and electropolishing to reduce dishing.

Embodiments of the present invention employ electrochemical principles, but in a reverse way, to strategically amend the corners. A conventional or simplified reverse process (plating) using conventional chemistries unfortunately is likely to be of limited utility, as the reverse process will only reverse the same field effect caused by the topography variations in the wafer and specifically the patterned dielectric

layer. That is, merely cycling between de-plating and plating for periods of equal duration or charge will produce no significant change in the within-feature dishing characteristics. In other words, the relative (corner vs. center of a feature) de-plating and plating rates in each step will be comparable. Embodiments of the present invention overcome these problems by changing the relative plating rate to obtain greater plating rate than the corresponding de-plating rate. In this way "corner mending" is performed.

FIG. 1 is a diagrammatic view of a trench using conventional electropolishing methods. As illustrated, the trench 102 shows signs of dishing. That is, within the feature (i.e., the trench) the level of the metal layer 103 is recessed in the corners 104 of the trench 102 as compared to the level of the metal 103 at the center 106 of the trench. This is believed to be caused by the relative differences in electropolishing rates. That is, the electropolishing rate 110 in the corners is greater than the electropolishing rate 111 in the center of the trench due to the presence of higher electric fields at the corners. Merely performing a cycle of deplating and plating is expected to produce only a negligible impact on the planarization effects since the plating rate 130 at the corners and the plating rate 131 at the center of the trench are expected to be approximately equal to the respecting deplating rates 110 and 111.

FIG. 2 is a diagram illustrating a trench polished in accordance with one embodiment of the present invention. This embodiment applies the approach of the topography-dependent plating to create greater acceleration (of plating) at the corners (within the local valley of the topography) as opposed to the plating at the center of a

feature or in the field area. That is, greater relative plating rates are induced at the corners of the features. The topography-dependant plating rates can be achieved by adding appropriate levels and types (size and functionality) of organic chemicals to the plating bath.

The expected effects of organic additives used during a pulsed recipe are illustrated in FIG. 2. The effects from the electropolishing (deplating) include dishing at the corners 204 of the trench 202. That is, the planarizing effect of the topography dependant recipe provides increased plating at the corners in comparison to conventional plating. The primary impacts from the pulsed recipe and the organic additives is illustrated in the localized plating rates. The de-plating rate 210 at the corners and at the center (211) are substantially the same as exhibited during conventional electropolishing. By including organic additives, such as accelerators and suppressors, plating rates change in a topography dependant fashion. The plating rates 230 at the corners of the feature are enhanced relative to conventional steps while the plating rate 231 at the center of the trench 202 remain relatively the same or are even reduced in accordance with an alternative embodiment. Thus, through the use of organic chemical additives, plating steps, and pulsed recipes, modification of the corner de-plating rate is achieved, with the result of improved planarization.

In accordance with a preferred embodiment of the present invention, the types of chemicals used include the following: (1) plating accelerators, (2) plating suppressors, and (3) the levelers. Plating accelerators are generally organic components that increase the plating rate. Suppressors, in turn, are organic additives

that suppress or decrease the plating rate for a given electric potential applied to the cathode and anode. Suppressors are typically large molecules with lower diffusion coefficients. These additives, for example, can produce beneficial effects in the plating and deplating of crevices due to differences in local concentrations. In particular, the local concentration of accelerators within crevices would be higher (than the "field" area) but lower in suppressors, resulting in higher plating rates in the crevices.

In some electroplating solutions, the levelers, which are larger molecules that also act to suppress plating, are added to produce a leveling effect, i.e., to compensate for the overplating (protrusion) over small features. Without wishing to be bound by any theory, it is believed that the levelers add little to the topography dependant plating, but may help reduce the relative corner de-plating, based on their greater attraction to the higher E-field area surrounding corners. Levelers may also hamper the corner plating rate for the same reason.

The plating accelerators are preferably relatively small and with relatively higher diffusion coefficients (relative to the suppressors or levelers) and, most preferably, are capable of enhancing the electron transfer at the electrochemical electrode for Cu plating. The suppressors (and levelers) conversely are preferably larger and with lower diffusion coefficients, and most preferably capable of creating a greater "double-layer" at the electrode's electrolyte-Cu interface. Suitable chemical additives are available commercially, including for example (1) Shipley 2 component chemistry, consisting only of accelerators and suppressors, (2) Shipley 3-component

chemistry, and (3) Enthone 3-component chemistry, the latter two including accelerators, suppressors, and levelers. Shipley chemical additives are available from Shipley Company, LLC of Marlborough, MA , whereas Enthone chemical additives are available from Enthone, Inc. of West Haven, Ct., a division of Cookson Electronics, PWB Materials and Chemistry Group of Londonderry, NH.

A variety of chemical compositions are available commercially for accelerators, suppressors, and levelers. For example, one available accelerator includes bis(3-sulfopropyl) disulfide (SPS). An available suppressor includes polyethylene glycol. One example of an accelerators is bis(3-sulfopropyl) disulfide (SPS), and for suppressor, polyethylene glycol. The preceding chemical additives are intended to be illustrative and not limiting. That is, there are many different variations in the chemical composition of suitable additives. With the guidance provided by this specification, one skilled in the art can be expected to identify suitable additives and concentrations with minimal experimentation.

It is anticipated that the local topography dependence of the accelerated rate will automatically adapt to a given local topography to bring about the desired level of compensation appropriate for any given topography. The accelerated plating is typically greater in smaller features as long as the feature size is not too small to impact the diffusion of the accelerator. The topography-dependence of the acceleration results in greater bottom-up fill. That is, improved gap fill is provided due to the tendency of the additives, specifically the accelerators, to accumulate at the corners of the trench, thereby acting as a catalyst for copper plating in those areas. In

other words, the deposition rate at the corners, including the bottom corners, is faster as compared to the rest of the surface to be plated.

In accordance with a preferred embodiment, a two-component chemistry (e.g., Shipley chemistry without a leveler) includes an Accelerator having a concentration in the range of 1 to 10 ml/L, and a Suppressor having a concentration in the range of 5 to 15 ml/L. In accordance with another preferred embodiment with a Leveler, i.e. a three-component chemistry (e.g., Enthone Chemistry), an Accelerator with a concentration in the range of 1 to 10ml/L, a Suppressor with a concentration in the range of 1 to 5 ml/L, and Leveler with a concentration in the range of 1 to 5 ml/L. are preferably provided.

FIG. 3 is a flowchart illustrating a method of polishing a substrate surface in accordance with one embodiment of the present invention. The recipe to induce corner mending process is preferably performed in a sequential processing flow, i.e., complete the de-plating step first, and then applying a reverse potential to induce corner mending. The preferred embodiment includes a sequence of "pulse" recipes that cycles through the de-plating and plating steps, with appropriately positioned "relaxation" step following the respective de-plating and plating steps. The purpose of relaxation step is to achieve local equilibrium before the next cycle begins. The ratio of the two sub-steps (deplating vs. plating) is preferably managed in a sequential manner, for example in one embodiment by progressively changing the de-plating to plating ratio in successive passes.

The process commences as illustrated in operation 302 with the deposition of a copper layer. As known to those of skill in the relevant arts, bulk copper may be deposited by conventional electroplating means, for example by immersing the semiconductor wafer in an electrochemical solution and depositing a bulk copper layer in the trenches. Next, as illustrated in operation 303, an optional partial CMP step is performed, particularly if the total Cu-deposition in the field area is greater than approximately 3000 Angstroms to induce reduction in surface roughness and to reduce the amount of Cu removal necessary at the electropolishing steps. Preferably, the CMP operation reduces the Cu to a field Cu thickness of approximately 2000 to 3000 Angstroms.

Next, as illustrated in steps 304 and 308, passes each comprising a series of deplating/plating/relaxation cycles are preferably performed with the substrate immersed in the plating solution by exposure of the wafer to the nozzle spray, the spray having the above described chemical additives in order to planarize the surface of the bulk copper. Commercially available stress-free polishers include types having a nozzle for spraying electrolyte in an upward direction to the wafer. The nozzle is also configured to move from center to edge, with electropolishing occurring in the general vicinity of the nozzle. Thus, according to a preferred embodiment, an initial pass 304 is preferably performed to initially quickly remove the exposed surface of the bulk copper. During this pass, the nozzle preferable moves from the center to the edge of the wafer. Accordingly, the initial pass commences in step 304, typically with the nozzle at the center of the wafer. After the initial pass is completed, planarization 308 continues. In accordance with embodiments of the invention, planarization step

308 then proceeds with the sequential deplating/plating/relaxation cycles , each cycle preferably commencing with deplating with additives, as illustrated in operation 308. Next, the plating step is performed to mend the feature corners, i.e., to plate the feature in a topography dependant fashion such that the localized plating rates at the corners of the feature such as the trenches are plated at an accelerated rate compared to the plating anticipated using conventional chemistries. That is, initially the plating rate using the electrolytes with additives is greater than the corresponding de-plating rate for the feature. Thus, the combined effects of the organic chemical additives provided in the plating solution provide plating in a topography dependant fashion.

Finally, each cycle or pulse of the many pulses performed during a pass completes with a relaxation step to allow local equilibrium to be reached before the next cycle begins. It will be appreciated by those of skill in the art that the degree (i.e., duration) of each of these steps (and sub-steps) depends on the diffusion coefficients of the various additives. Once the cycle is completed (at the relaxation step) a new cycle of deplating, plating, and relaxation commences, the cycles performed repeatedly until the pass is completed, e.g., the nozzle has reached the edge of the wafer in one embodiment. Preferably, the duration of each of the sub-steps in the cycle (i.e., plating, deplating, relaxation) falls within the range of milliseconds to tens of milliseconds, i.e., 1 ms to 100 ms. Thus, in accordance with this embodiment, each pass would comprise many cycles (e.g., thousands) as the nozzle moves along the wafer.

After the pass is completed, a determination 312 is made as to whether further passes are needed, i.e., whether planarization has been completed. If further passes are needed, the ratio between de-plating and plating may be adjusted in step 314 and the operation 308 (i.e., plating w/additives, deplating w/ additives, and relaxation) repeated to achieve the desired effects. Once the desired planarization is achieved, the process ends.

In a preferred embodiment, the ratio of the de-plating rate to the plating rate is controlled in accordance with the progress in planarizing the bulk deposited copper. For example, in accordance with one embodiment, the ratio between de-plating and plating is initially set to be much greater than 1 when a "continuous" Cu layer is present. This will achieve needed overall stress free polishing in a time efficient manner. As the barrier surface begins to be exposed, this ratio is preferably gradually decreased toward 1.0 and reaches 1.0 when the Cu level reaches the desired Cu dishing characteristics in the features. Finally, the duration of the de-plating/plating ratio of 1.0 can be extended to achieve the desired planarity effect.

In an alternative embodiment, after each pass in a plurality of passes, the de-plating/plating ratio is adjusted progressively from the initial value to a final value approximating 1.0. The chemical levels of the organic additives can change based on the recipe. The relaxation period duration is preferably dependant upon the diffusion coefficients for the additives used. The range of concentrations for the additives depends on the feature size. Preferably, the de-plating/plating ratio initially is about 1.5 and gradually is decreased to about 1.0 to 1.1. Preferably, when a desired surface

topography is reached, the de-plating/plating ratio is set to about 1. In accordance with yet another alternative embodiment, the initial pass is adjusted such that only deplating occurs.

In summary, to apply varying deplate-to-plate ratios, "multiple passes" along the wafer are made, with one recipe per pass for consistency of the whole wafer. Since the duration of the deplate-plate-relaxation cycle is very short, as stated above, many cycles would result as the nozzle moves along. Optimal concentrations of the chemical additives can be determined with minimal experimentation. For example, initial concentrations can be selected to correspond to concentrations typically used for electroplating since that portion of the recipe would be used to mend the corners.

According to one embodiment, the first pass (nozzle moving from center to edge) of the electropolishing uses either a no pulse recipe (i.e., deplating without a plating step in the cycle) or a pulsed recipe (i.e., deplating, plating, and relaxation) with high deplate-to-plate ratio, until the Cu thickness in the field area is very low or when the underlying barrier layer begins to be partially exposed. Then in the second (or additional) pass(es) a pulsed recipe with a low (or lower) deplate-to-plate ratio(s), is used. The number of passes will depend on optimization of the process but preferably the number of passes are minimized.

The process described above using a spray nozzle configured to move from center to the edge of the wafer is intended to be illustrative and not limiting. That is, the scope of the invention is intended to extend to all electropolishing tools. For example, other electropolishing tools include "wafer-wide" types (i.e., "fountain type

of cells" with no nozzles, whose electrolyte would cover all wafer area at once like conventional electroplaters), and the sequence of steps illustrated in FIG. 3 can be adapted to correspond to the type of electropolisher. That is, the application of multiple pulsed recipes can be controlled by software to adjust the rates after the completion of each pass. It is understood that using the wafer wide electropolishing tool, a pass would not refer to the movement of the nozzle but instead to a particular pulsed recipe.

Preferably, but not intended to be limiting, the current density provided to the anode and cathode in the plating solution is optimized to effect a removal rate of 1000-2000 Angstroms per minute by the combination of de-plating and electroplating and relaxation. The electropolishing rate, and, in turn, the plating rate may be controlled by one or more of the current density (voltage) and the duration of the step. These parameters are pattern density dependant.

It is expected that a control unit may be suitably configured, according to one embodiment, to respond to various input signals (including degree of planarization, timing signals and signals for endpoint detection) that may be developed by those of skill in the art to direct the sequence of de-plating/plating/relaxation cycles.

The controller is preferably configured to adjust the de-plating/plating ratios such as the duration of the individual sub-steps (e.g., the plating, deplating and relaxation during step 308) as well as the number of cycles to achieve the desired degree of planarization. That is, the controller may be configured to apply or remove

voltage or current from the anode and cathodes in the plating solution or reverse the currents to change the operation from de-plating to plating and vice versa.

While the above sequences of electropolishing and plating steps in combination are preferable, the invention is not so limited. The rates of polishing and plating during each pass (i.e., the series of complete plating, deplating, and relaxation cycles), the number of passes, and the variation from pass to pass are not specifically limited, but dependant upon the particular layer sought to be removed, the topography of the layer, and whether a high removal rate or fine polishing is desired. As a further example, in one embodiment, for each pulse or cycle, the plating may precede the deplating and still be in keeping with the spirit and scope of the present invention.

The embodiments of the present invention have generally been described with reference to a copper damascene structure but should not be interpreted as limiting the invention. It should be appreciated that the embodiments of the present invention may be adapted to work with the polishing of different metals, both in damascene structures and in other layers.

The techniques of the present invention provide the capability to polish copper layers on wafers having low-k films without damaging the structure. High removal rates can be achieved by controlling the current and voltage to the wafer during initial polishing, and ensuring planarity by reducing the ratio of polishing to plating during subsequent cycles, for example commencing at the time the substrate is first exposed. The process thus results in a stress free or low stress planarization. The polishing system may be implemented by minor modifications to existing hardware such as by

including control circuitry to reverse the current to the electrodes in a precision time controlled fashion.

The use of additives as disclosed herein also provides additional methodologies to address Cu residue issue that might occur in field areas. Specifically, by using a pulsed recipe with deplating to plating ratios just above 1, one can achieve overall deplating in the field area (the plating/deplating rates would be equivalent since there is no topography) to eliminate/reduce the Cu residues. The impact of deplating to plating ratios just above 1, for organic additive-less electrolytes would typically result in increased dishing in the features as well. However, the "bottom-up" fill (resulting from the topography-induced concentration gradient) will compensate for this deplating to plating ratio, and thereby- maintain/minimize the dishing in the feature.

Although the foregoing invention has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims.